

ABSTRACT

Methods and systems for managing control structure access by a
5 processor are disclosed. In general, a processor can communicate with a
plurality of control structures. A memory window manager can then be
implemented, which communicates with said processor and said plurality of
control structures. The memory window manager specifies which control
structure among said plurality of control structures is accessible by said
10 processor. The memory window manager also specifies which control structure
can be mapped into an address space of said processor.